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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,954	01/05/2004	Takao Aigo	8001-1178	2049

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EXAMINER

KROFCHECK, MICHAEL C

ART UNIT	PAPER NUMBER
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2186

DATE MAILED: 05/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/750,954	Applicant(s) AIGO, TAKAO	
	Examiner Michael Krofcheck	Art Unit 2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 January 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4 and 6-9 is/are rejected.
- 7) ☒ Claim(s) 5 and 10 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05 January 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 5/23/2006.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

1. This office action is in response to application 10/750,954 filed on 1/5/2004.
2. Claims 1-10 have been submitted and examined.

Priority

3. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). Receipt is acknowledged of the certified copy submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

4. The information disclosure statement filed 1/5/2004 fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not in the English language. It has been placed in the application file, but the information referred to therein has not been considered.

The concise explanation of the relevance needs to be spelled out within the IDS or included documents such as a translated abstract and statement of relevance included with the foreign patent document. The reference to the applicant's specification wherein the two foreign documents are merely cited as examples and not themselves explained does not satisfy this requirement.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 6 rejected under 35 U.S.C. 102(b) as being anticipated by O'Neil et al., US patent 6085287.

7. With respect to claims 1 and 6, O'Neil teaches of a disk array control apparatus/method comprising: a first element constructed and arranged so that the first element calculates a cache hit ratio at a disk cache memory (fig. 2; item 26; column 3, lines 55-57); and

a second element constructed and arranged so that the second element adjusts a number of tasks to be executed according to the calculated cache hit ratio (fig. 2; item 28; column 4, lines 34-39).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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9. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claims 2 and 7 rejected under 35 U.S.C. 103(a) as being unpatentable over Bala US patent 6351844, and O'Neil.

11. With respect to claims 2 and 7, Bala teaches of a first element constructed and arranged so that the first element calculates a cache hit ratio at a cache memory (column 8, lines 34-46; as the cache hit rate is used in determining a threshold; there must be an element that calculates it); and

a second element constructed and arranged so that the second element decreases a number of tasks to be executed when the calculated cache hit ratio is above a prescribed value and increases the number of tasks to be executed when the calculated cache hit ratio is below the prescribed value (column 8, lines 34-46; if the cache hit rate is high, the threshold is raised so no more traces are examined (lower number of tasks). If it is low, the threshold is lowered so that an increasing number of traces are examined (higher number of tasks). Since the cache hit rate being high or low is used to vary the threshold, there must be a cache hit rate threshold that signifies a high or a low cache hit rate).

Bala fails to explicitly teach of a disk cache memory. However, O'Neil teaches of a disk array control apparatus/method comprising: a first element constructed and arranged so that the first element calculates a cache hit ratio at a disk cache memory (fig. 2; item 26; column 3, lines 55-57).

It would have been obvious to one of ordinary skill in the art having the teachings of Bala and O'Neil at the time of the invention to implement the cache system identifying hot traces of Bala in the cache memory system of O'Neil. Their motivation would have been to efficiently identify the hot traces to capture the current working set in the cache memory (Bala, column 8, lines 38-40).

12. Claims 2-4 and 7-9 rejected under 35 U.S.C. 103(a) as being unpatentable over Ryan US patent 5367656, and O'Neil.

13. With respect to claims 2 and 7, Ryan teaches of a first element constructed and arranged so that the first element calculates a cache hit ratio at a cache memory (fig. 1, 5; column 2, lines 58-63); and

a second element constructed and arranged so that the second element decreases a number of tasks to be executed when the calculated cache hit ratio is above a prescribed value and increases the number of tasks to be executed when the calculated cache hit ratio is below the prescribed value (fig. 1, 5; column 8, lines 63-column 9, line 7).

Ryan fails to explicitly teach of a disk cache memory. However, O'Neil teaches of a disk array control apparatus/method comprising: a first element constructed and

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arranged so that the first element calculates a cache hit ratio at a disk cache memory (fig. 2; item 26; column 3, lines 55-57).

It would have been obvious to one of ordinary skill in the art having the teachings of Ryan and O'Neil at the time of the invention to include the cache predictive prefetching system of Ryan in the cache memory system of O'Neil. Their motivation would have been to lower the cache miss ratio (Ryan, column 2, lines 40-42).

14. With respect to claims 3 and 8, Ryan teaches of a first element constructed and arranged so that the first element calculates a cache hit ratio at a cache memory (fig. 1, 5; column 2, lines 58-63);

and a second element which executes only high priority tasks when the cache hit ratio is above a prescribed value and executes both the high priority tasks and low priority tasks when the cache hit ratio is below the prescribed value (fig. 1, 5; column 3, line 51-column 4, line 14; column 8, lines 63-column 9, line 7; when the hit ratio is below the threshold, the miss prediction is enabled, so that miss prediction occurs and regular cache accessing occurs. The regular cache accessing by the main processor, i.e. the main processor requesting operands/data from the memory, etc, are high priority tasks since they are required for processor to carry out the program. The miss prediction is a low priority task because it just enhances the performance of the cache memory, it is not required for the main processor carry out the program. When the hit ratio is above the threshold, the miss prediction is disabled, and so only the tasks from the processor are carried out).

O'Neil teaches of a disk array control apparatus/method comprising: a first element constructed and arranged so that the first element calculates a cache hit ratio at a disk cache memory (fig. 2; item 26; column 3, lines 55-57).

15. With respect to claim 4, Ryan teaches of a high priority I/O process execution unit constructed and arranged to allow execution of high priority tasks (fig. 1-2; column 4, lines 7-14; as the request for an operand (high priority I/O task) results in a hit or miss, and further processing of the request, there must be a processing unit that does this);

a low priority I/O process execution unit constructed and arranged to allow execution of low priority tasks (fig. 3-5; column 7, lines 50-63; where the miss prediction process (low priority I/O task) is enabled or disabled by the result of comparing the hit ratio with the hit ratio threshold);

a cache hit determination unit constructed and arranged to determine whether or not the I/O process request is causing a cache hit at a cache memory (fig. 2; column 4, lines 7-14);

a cache hit ratio monitor unit constructed and arranged to calculate and output a cache hit ratio within some period of time by using a determination result of the cache hit determination unit (fig. 1, 5; column 2, lines 58-63; as it must be known if the request is a cache hit or miss to calculate the ratio, the hit ratio must be calculated based on whether the requests were hits or misses in the cache memory); and

an execution task selection unit constructed and arranged to allocate each said I/O process request to either the high priority I/O execution unit or the low priority I/O

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process execution unit (fig. 1, 3-5; column 4, lines 7-14; upon the operand/data request, the request are sent to determine if they result in a cache hit or miss (high priority I/O execution unit)),

the execution task selection unit activating only the high priority I/O process execution unit when the cache hit ratio is not less than some prescribed value and activating both the high priority I/O process execution unit and the low priority I/O process execution unit when the cache hit ratio is less than the prescribed value (fig. 1, 5; column 3, line 51-column 4, line 14; column 8, lines 63-column 9, line 7; when the hit ratio is below the threshold, the miss prediction is enabled, so that miss prediction occurs (low priority I/O execution unit) and regular cache accessing occurs (high priority I/O execution unit). The regular cache accessing by the main processor, i.e. the main processor requesting operands/data from the memory, etc, are high priority tasks since they are required for processor to carry out the program. The miss prediction is a low priority task because it just enhances the performance of the cache memory, it is not required for the main processor carry out the program. When the hit ratio is above the threshold, the miss prediction is disabled, and so only the tasks from the processor are carried out (high priority I/O execution unit)).

O'Neil teaches of a disk array control apparatus comprising: a host I/O reception unit arranged so that the host I/O reception unit receives as an input an I/O process request from a host computer and analyzes the I/O process, the I/O reception unit generating as an output the I/O process request (fig. 2; item 22, column 3, lines 54-65) and a disk cache memory (fig. 2; item 18);

16. With respect to claim 9, Ryan teaches of a control method comprising the steps of: inputting an I/O process request from a host computer (fig. 2; column 4, lines 7-10);

determining whether the I/O process request is causing a cache hit at a cache memory (fig. 2; column 4, lines 7-14);

calculating a cache hit ratio within some period of time based on results of the determining step (fig. 1, 5; column 2, lines 58-63; as it must be known if the request is a cache hit or miss to calculate the ratio of such, the hit ratio must be calculated based on whether the requests were hits or misses in the cache memory);

identifying the I/O process request as either a high priority task or a low priority task (as the process of requesting an operand has been issued by the processor, and it is needed by the processor to execute the program, it is abundantly clear to one of ordinary skill in the art that it is a high priority task. . Mason, Jr. et al., US patent 6,557,079, provides additional support for this (column 10, line 64-column 11, line 13));

executing only high priority tasks when the cache hit ratio is not less than some prescribed value; and executing both high priority tasks and low priority tasks when the cache hit ratio is less than the prescribed value (fig. 1, 5; column 3, line 51-column 4, line 14; column 8, lines 63-column 9, line 7; when the hit ratio is below the threshold, the miss prediction is enabled, so that miss prediction occurs and regular cache accessing occurs. The regular cache accessing by the main processor, i.e. the main processor requesting operands/data from the memory, etc, are high priority tasks since they are required for processor to carry out the program. The miss prediction is a low priority task because it just enhances the performance of the cache memory, it is not required

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for the main processor carry out the program. When the hit ratio is above the threshold, the miss prediction is disabled, and so only the tasks from the processor are carried out).

O'Neil teaches of a disk array control method comprising: calculating a cache hit ratio within some period of time at a disk cache memory (fig. 2; item 26; column 3, lines 55-57).

Allowable Subject Matter

17. Claims 5 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Mason, Jr. et al., US patent 6,557,079 teaches data reads and writes being high priority tasks, while prefetching is a low priority or background task.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C. Krofcheck whose telephone number is 571-272-8193. The examiner can normally be reached on Monday - Friday.

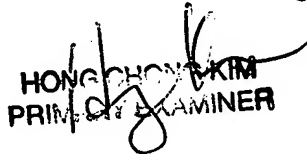
20. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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21. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Michael C. Krofcheck



HONG CHON KIM
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